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Planarization Technology to Promote Super LSI Integration

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Preface

94FE0802A Tokyo JAPAN SOCIETY FOR PRECISION ENGINEERING in Japanese 16 Jun 94 pp cover and i

[Lecture No. 205, held June 16, 1994 (Thursday), at Ie no Hikari Hall; sponsored by the Japan Society for Precision Engineering Planning/Business Committee in cooperation with: Society for Applied Physics, Society for Instrumentation and Automated Control, Data Processing Society, SEMI Japan, Electrical Communications Association, Society for Electronic Data Communications, [Abrasive Grain Processing] Society, Japan Chemical Society, Japan Machinery Society, Japan Machinery Industrial Association, Japan Optical Instrumentation Industrial Association, Japan Semiconductor Production Equipment Association, Japan Precision Instruments Industrial Association, Society for Printed Circuitry, [Reed] Exhibition Japan, Laser Society]

[FBIS Translated Text] The Japanese semiconductor industry assumed the world lead when the 256K DRAM came into existence, based on excellent production technology. However, U.S. manufacturing companies are better in production of the MPU; and Korean companies have caught up in production of the 16M DRAM. Japan is beginning to lose its leading position.

Much effort has been exerted toward the integration of VLSIs in an attempt to regain Japan's front position, and new problems associated with this development have come into existence.

For example, the need for multilevel wiring increases with the shift toward smaller design rules in the VLSI, resulting in the need for planarization technology for the interlayer insulating film. Various planarizing methods have been tested, such as precision polishing which utilizes a mechano-chemical reaction.

In this lecture, the current status of planarization technology, which is essential to integration of the VLSI, will be discussed. In addition, this lecture will cover the necessity for planarization with regard to device design and lithography, and the newest techniques such as defocus exposure method, ultra-precise polishing, machining, and cleaning techniques.

I would like to express my appreciation to all of those in attendance and also to all those who contributed on my behalf.

June 16, 1994

Precision Engineering Society Business Committee Planning Committee, Group 5

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Present Status and Future Outlook of Planarization Technology

94FE0802C Tokyo JAPAN SOCIETY FOR PRECISION ENGINEERING in Japanese 16 Jun 94 pp 1-5

[Lecture by Arita of the NTT LSI Research Center]

[FBIS Translated Text]

[1] Introduction

Modern industrialization has brought to society innumerable benefits, but at the same time has produced many problems. This is not the society we all desire. We are at the end of a generation and in a transitory period, heading for a new era. The next generation will be created by new sciences and technologies. Although still in its preliminary stages, the next generation technologies are beginning to take shape.

At issue are the building of systems which achieve a balance between hardware and software technology, while creating revolutionary systems based on long-term global standardization. In addition, business development practices are in question. There has also been a long-standing clamor for long-term global reform with far-reaching effects on Japanese industry, government, education, and social structure.

The fact that large-scale integration is one of the hardware-related key technologies will not change in the future. The LSI cost/benefit ratio continues to improve in conjunction with proportional size reduction rule. By the beginning of the 21st century, we can expect chip performance to be 10 times better, and system performance will likely be 100 times better. This is based on the trend toward subminiaturization and higher integration. Although improvement is all good and well, there are some drastic reforms which are needed to overcome the associated problems. One of these problems is that the LSI fabrication processes are becoming too complex. With successive generations, the number of processes required also increases, and the costs associated with development and equipment have also reached their limit. This is why more effective technology is needed to facilitate production of the LSI, or to enable process feedback by thorough in-situ process monitoring.

To achieve logic LSIs with higher integration levels in the future, more than the current 3-4 levels of wiring is required. Five to seven levels of wiring can be expected, along with the development of CAD wiring layout techniques. Memory LSIs will also increase in wiring levels, from two layers at present to three layers. In achieving this multilevel wiring, the resolution of subminiature patterns, formed by excimer exposure devices which use short wave-length light sources, is greatly affected by the unevenness of the sublayer. This is why global type planarization of devices and wiring steps is essential.

In the past, a combination deposition/etchback method has been used for global smoothing and planarization. However, chemical/mechanical polishing has recently come into use; in some cases, this has been used for planarization of LSIs in mass production systems. Some functions used in in-line LSI production processes include: deposition, cleaning, etching, heat processing, oxidation, ionic injection, and exposure processes. Polishing to achieve planarization has also been added.

This discussion will summarize the current status and problems, and the future outlook for smoothing and planarizing technologies.

[2] Types of Planarizing and Smoothing Techniques

The planarizing and smoothing techniques which have been used to date can be roughly classified into the following four types. (See Figure 1)

(1) In-situ flow during film growth, reflow by post-anneal following film formation.

1. Smoothing and planarizing of insulating films and metals by in-situ flow.
2. Smoothing and planarization of insulating films and metals by post-anneal reflow.

(2) Selective deposition.

1. Planarizing of single crystal silicon, polycrystal silicon, metals, and insulating films by selective deposition.

(3) Film formation and etching.

1. Smoothing and planarizing by etchback, which is a combination of film growth and etching.
2. Smoothing and planarizing by in-situ film growth and etching.

(4) CMP

1. Smoothing and planarizing of silicon, polycrystal silicon and insulating film by chemical/mechanical polishing.

All of the above methods have advantages and disadvantages, and the appropriate method should be selected from an overall point of view.

Figure 1. Classification of Smoothing and/or Planarization Method

Methods	Selective or Blanket	In- or Ex-Situ	Element Processes	Materials: Insulator, Single Si, Poly Si	Materials: Metal
Deposition	Blanket	In situ Flow	Coating		
			PVD		
			CVD		
		Sequential ,Reflow	Coating		
			PVD		
			CVD		
	Selective	In situ	Plating		
			CVD		
Deposition and Etching	Selective and Blanket	Sequential	Coating, CVD		
		In situ	Bias PVD		
			Bias CVD		

[3] Problems Associated With the Etchback Method

Some typical production processes include: smoothing by BPSG (low temperature reflow), global smoothing or local planarization of insulating film by using a combination of etchback with P-CVD SiO_2 film and organic or inorganic SOG coated film. In recent years, planarization has been done by selective CVD of metals for subminiature contacts and via holes with high aspect ratios, and metal embedding by blanket CVD. However, the following problems are associated with these methods.

1. With coated thick films such as resist and SOG (organic and inorganic), the roughness of the sublayer pattern is easily affected. For example, it is difficult to achieve complete flatness at a point 10μm or more away from the edge of a step pattern in the horizontal direction.
2. Thick-coated film on a sample having pattern steps; the etchback surface uniformity is a sum of the uniformity within the surface of thick-coated film or CVD film and the uniformity of the etchback rate during reactive ion etching.
3. The process margin for constant rate etchback is small.
4. Metal, silicon, and poly-silicon etchback is easily affected by microloading.

[4] Background of Complete Planarization

As for methods which use global smoothing and local planarization by a combination of conventional techniques, for multilevel wiring of large scale logic LSIs which will require even more layers of wiring than presently used, we will soon reach the limitations associated with higher yield, less complexity, and lower cost, for the following reasons:

(1) It will be essential to use more layers of wiring (five to seven) to achieve higher levels of integration and faster operating speed. When wiring layers are stacked, there is a wire step that is one micron or larger. The step is also very steep; and the physical formation of the wire itself is difficult to achieve by sputtering.

(2) The focal depth of lithographic methods which use short wavelength KrF and ArF excimers is about one micron or less; if a step is larger than the focal depth, the pattern will not be easily formed due to the resolution limitation.

(3) When there is a steep step, there is no process margin for reactive ion etching of subminiature wires, and the wire reliability is less.

(4) There is increasing demand for the degree of CAD freedom in CAD design of the circuit layout, such as for contacts, via-holes, and circuit lines.

(5) Production equipment will have to accommodate several generations of products at the same time. This will also be true of planarization. Once local and global planarizing methods are established, they will be standardized for future LSI multilayer wiring methods, enabling the simultaneous production of many product generations.

Based on the above technical background, there is a need for local and global planarizing techniques.

[5] Complete Planarization Process Steps and Key Technologies

As shown in Figure 2, applications for complete planarization can be roughly classified into device, isolation, and interconnection processes. Typical areas in MOS devices which require planarization are convex areas in gate polysilicon, convex areas in LOCOS Si thermal oxide film, or CVD SiO_2 film used for device isolation. Sputtered areas for embedding contact and via-holes, and convex areas of metal CVD film also need to be flattened.

There are three key technologies needed for planarization:

(1) Complete filling:

Complete and voidless filling of materials such as insulating film used for subminiature spaces, trenches, and holes having high aspect ratios, metals, single crystal silicon, and polysilicon.

(2) Higher quality filling materials and control of film properties:

Deposition should be possible at low temperatures, and there should be little hydrogen or water content in the insulating film; the materials should have a low dielectric constant, low stress and high resistance, to cracking. Also, metals should adhere better to sublayer insulating film; and they should be low in electrical resistance, highly resistant to stress and electromigration, and low in stress.

(3) Borderless planarization:

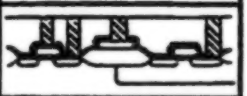
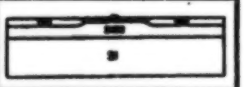
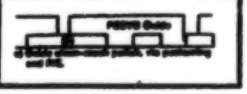
Film which has been deposited outside of the prescribed areas is eliminated, and the insulating film, single crystal silicon, polysilicon, and metals are planarized in a "borderless" manner.

[6] Application of CMP, Positioning, and Associated Problems

The mechano-chemical polishing technique, which was initially known in the latter half of the 1960s as the EPIC technique, and which has now become an established production technique for silicon wafers, is used to polish single crystal silicon to achieve complete isolation. In the early 1970s, polysilicon polishing for V groove filling was used for planarization and device isolation of high speed SRAMs. In the latter half of the 1980s, it was used for polishing single crystal SOI silicon for adhesion. In addition, CMP processes have been reported which are suitable for planarizing after shallow trench device isolation and metal hole embedding have been performed, using a high precision polisher with computer-controlled polishing parameters.

CMP technology, like etchback, can be used for three fabrication processes—device planarization, isolation,

Figure 2. CMP Applications to Planarization

Application Processes	Targets	Materials	Structures
Device	Recess of convex parts in device active region	Poly-silicon, ...	
	Planarization of convex parts in device active region	Insulator(SiO2, ...)	
Isolation	Trench and V-groove isolation	Insulator(SiO2, ...) Poly-silicon, Single silicon	
	Silicon on Insulator	Single silicon(Wafer bonding), Poly-silicon	
Interconnection	Recess wiring	W,Al,Cu	
	Plug formation	W,Al,Cu	
	Multi-level dielectric planarization	Insulator(SiO2, ...)	

and wiring. Five examples of CMP applications are shown in Figure 1 [sic]. Some materials which can be polished are single crystal silicon, poly-silicon, insulating film (SiO_2), and metals (tungsten, copper, and aluminum).

1. Polishing of polysilicon to create recessed gates which are convex areas in MOS devices.
2. Planarization of insulating film to eliminate level differences between MOS gates and LOCOS before entering the wire fabrication process.
3. Polishing of single crystal silicon and polysilicon in trenches which are used for device isolation.
4. Eliminating tungsten nuclei when selectivity breaks down during hole embedding, when W selective CVD is used to form plugs; and polishing of aluminum after reflow by tungsten and copper blanket CVD, flow sputtering or post annealing.
5. Planarization of metals used to form recessed type embedded wiring.
6. Polishing of interlayer insulating films in multilevel wiring.

Compared to the etchback technique, in CMP technology there is a larger margin for over-etching and less effects attributed to microloading. CMP is also regarded as an effective tool in terms of resolving several problems related to the etchback method. However, the following issues must be studied with regard to CMP.

(1) CMP of insulating films:

1. When polishing insulating films, the polishing rate is easily affected by level differences between devices, size of the device pattern, and roughness. Reproducibility of the CMP rate, improved uniformity, and dependency on the pad surface should be examined.
2. After polishing is performed, there is physical scratching on the surface of the insulating film; and mobile ions, other cluster ions (for example, Si_2O_6H-), and slurry are present. Therefore, a post-processing step, such as wet surface etching or surface cleaning, must be performed.
3. CMP in-situ completion detection. One means of detecting polishing completion for materials of differing hardness is by converting the AC current which flows to the motor of the pad rotation mechanism to DC, and then processing the signal. This is a practical method of monitoring the progress of polishing, and has already been commercialized. However, this method is not effective when hardness levels are similar.
4. Control of global planar uniformity within the surface, a problem caused by curvature of the wafer which occurs during processing; and increased tolerance for this curvature.
5. Use of a polishing stopper layer.

(2) Chemical/mechanical polishing of metal films:

1. During chemical/mechanical polishing of metals, the polishing rate is easily affected by unevenness of devices, the size of patterns, and the amount of roughness; therefore, dishing and thinning frequently occur.
2. Soft metals, such as aluminum and copper, are more susceptible to surface scratching by CMP than hard materials such as tungsten.
3. Rust-type corrosion on metal film surface.
4. Stress cracking when adhesion between metal and insulating films is weak.
5. When slurry containing silica is used, the silica frequently seeps into the metal.
6. In-situ completion detection.
7. Polishing stopper layer is needed.

(3) Treatment of the insulating film surface after polishing:

After polishing, there is slurry residue, physical scratching, mobile ions, and other ionic adhesion. Therefore, a wet-type cleaning or some other treatment is needed for the surface.

(4) Description of the CMP planarization mechanism.

It is important to understand the mechanism which occurs between the pads, slurry, metals, and insulating films. A process simulation which begins from the first principle, and a model for CMP process design should be established in the future.

(5) Compared with conventional chemical and physical type methods, CMP holds the following position:

1. Planar process margin should be larger.
2. Planarization process should be simpler.
3. Next-generation high performance processes should be developed.

[7] Future Outlook for Planarization Technology

The mechano-chemical polishing (MCP), or in other words, the CMP method, has become established as a mirror surface polishing technique since the creation of semiconductor LSIs. It is now being reconsidered as an LSI in-process global planarization technique, and has begun to be used for this purpose. It is used for planarization of chip-level devices, device isolation, SOI, wiring, and other applications. As it has not been long since in-process MCP, or CMP, has come into being, in order to design processes and achieve easy-to-use processes, a

detailed scientific understanding of the phenomenon is needed. In addition, to achieve high precision process control, a process model and simulation techniques should be developed. A more portable, easy-to-use type of polishing device is also needed.

With regard to planarization by physical and chemical methods, a larger process margin, much simpler processing, and creation of processes which have new added value will be the building blocks for future development of CMP technology.

As we are unsure of what lies ahead in the next generation, we have come to a point where conventional ways of thinking must be reconsidered with regard to research and development and mass production efforts in various industrial fields. The semiconductor LSI industry is no exception. The customer will continue to seek module-based systems which have true value, general purpose applications, and no disadvantages. In the long range, such systems should be based on worldwide standards.

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Planarization Using Defocus Exposure Method

94FE0802D Tokyo JAPAN SOCIETY FOR PRECISION ENGINEERING in Japanese 16 Jun 94 pp 6-9

[Lecture by Masahiko Nakamae of the NEC ULSI Device Development Laboratory]

[FBIS Translated Text]

1. Introduction

It is very important to promote more levels and smaller levels of wiring in logic devices such as microprocessors and ASICs, which provide various complex logic functions on a chip with limited dimensions. Using conventional exposure technology and dry etching as the driving force behind subminiature processing technology, highly integrated chips with 1,000,000 gates have been developed.

In advancing the subminiaturization of wiring even further, several items regarding the planarization of interlayer films have come into view. One is that the focal depth in stepper exposure becomes smaller with size reduction, and it is becoming difficult to form subminiature patterns over the entire surface of the chip. This is why achieving a flat surface over the entire chip is crucial. In terms of the device, the resistance between two points of a wire formed on a bumpy surface is higher than on a flat surface, leading to poorer operational speed of the LSI. The parasitic capacitance associated with the wire on a bumpy surface is also higher than the one on a flat surface, and this also causes poorer operational speed. It is also important to consider the fact that local stress is present in the bumpy areas.

In this report, a global planarization technique will be introduced, using a relatively simple method that utilizes the defocusing exposure properties of photoresist.

2. Process

This process is called the DRESS (defocused resist patterning with blanket stripe mask) method. It consists of forming a stripe pattern of resist at the bottom of the step area, and using this pattern in an etchback process.

Formation of the stripe pattern will be discussed first. Figure 1 is a cross-sectional diagram showing the chief processes involved in the planarization of interlayer film. A step difference of 0.6μm to 3.1μm is created, using a multilevel wire design of up to four layers. After forming the last wire layer, the plasma oxide film is formed at a film thickness that is greater than the step difference. Then, resist is applied at a thickness equivalent to the step difference. Next, the stripe pattern is created on the resist by stepper exposure. By changing the line width and gap in the stripe mask, and by varying the focal position, the focal point can be set at the bottom of the step difference. The resist at the upper part of the step difference is removed, and the stripe pattern remains only at the bottom.

The etchback process is performed next. Both the resist etchback method and the oxide film etchback method will be described.

(1) Resist etchback method

A cross-sectional diagram of this method is shown in Figure 1(a). A second layer of resist is applied on top of the shapes formed by the DRESS method for planarization. For the etchback, ECR etching with CF_4 gas was used. Selectivity between resist and oxide film was almost 1.

(2) Oxide film etchback method

A cross sectional diagram of this method is shown in Figure 1(b). The resist pattern achieved by the DRESS method is used as a mask, and oxide film is etched to a depth equivalent to the original step difference. After the resist is removed, plasma oxide film is formed at a thickness equal to about half the gap between the stripes. SOG is then applied for planarization.

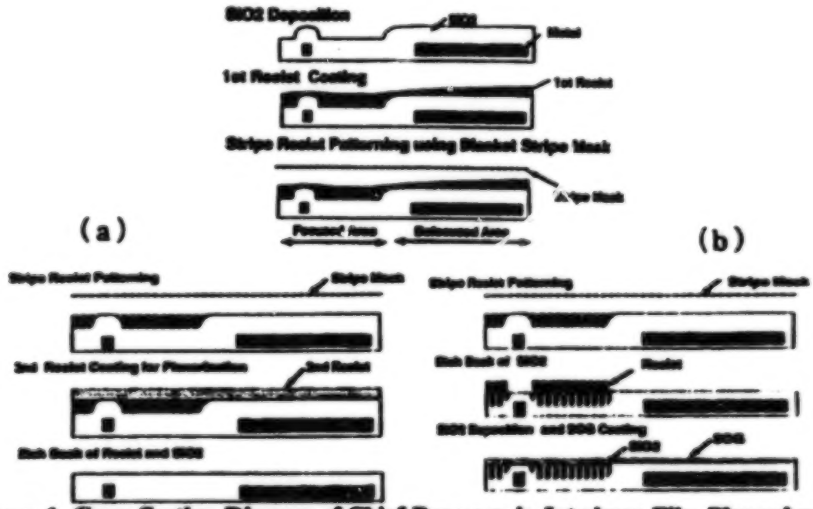

Figure 1. Cross Section Diagram of Chief Processes in Interlayer Film Planarization

3. Test Results

First will be discussed the exposure conditions needed to form the stripe pattern. Figure 2 [not reproduced] is a cross-sectional SEM photograph of the exposure results for two types of focal positions and a step difference of 3.1μm. The figures show that the desired shape is achieved where the focal point is set for the bottom of the step. Figure 3 shows the correlation between stripe width and focus offset. Under these conditions, the focus window, where only the stripe pattern at the bottom of the step remains, is from 1μm to almost 3μm. Figure 4 shows the correlation between the surface step difference following resist etchback, and the focus offset. The surface step difference within the range of the focus window (Figure 3) is reduced about 25 percent compared to the condition prior to planarization. For effective planarization, a resist film thickness that is equivalent to the step difference prior to planarization is required. As the step difference increases, the resist film thickness increases, and the resolution of the resist decreases. Therefore, it is necessary to also increase the size of the stripe mask.

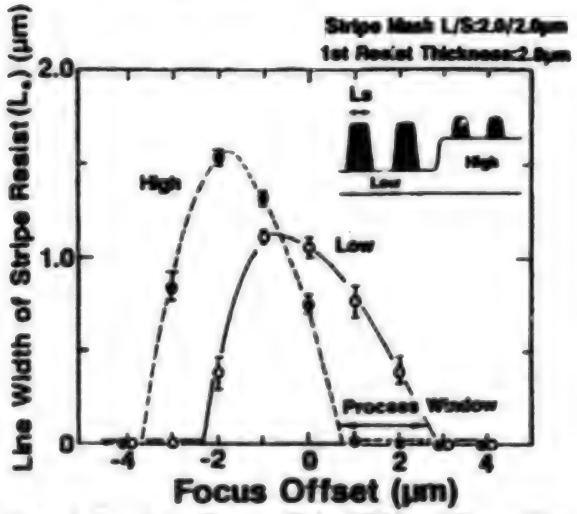

Figure 3. Correlation Between Stripe Width and Focus Offset

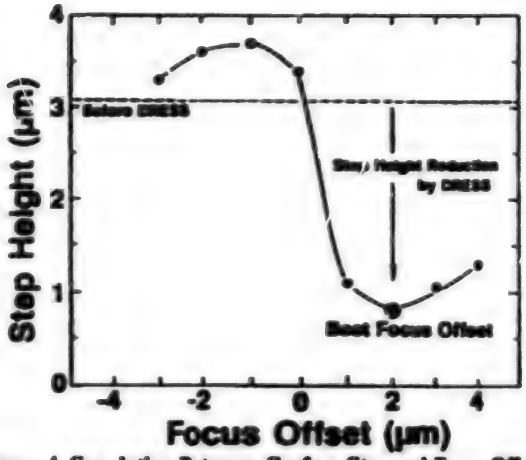

Figure 4. Correlation Between Surface Step and Focus Offset

second resist. Figure 7 [not reproduced] shows the condition after resist etchback has been performed. Both localized and global flatness are very good.

Next, the results pertaining to the oxide film etchback

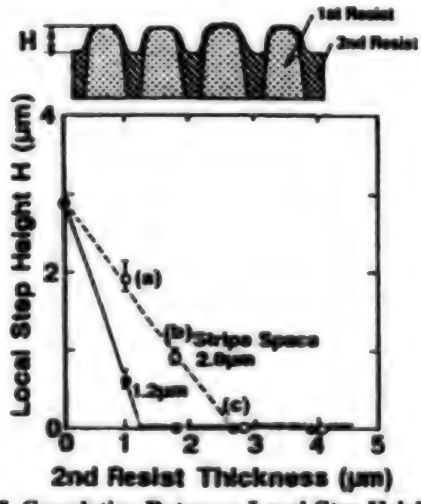

Figure 5. Correlation Between Local Step Height and Second Resist Thickness

The results of the etchback process will be reviewed next. The results of resist etchback will be described first. Figure 5 shows the correlation between localized step differences following applications of the second resist, and the film thickness of the second resist. The localized step differences disappear as the film thickness increases. Since this is good for embedding as long as the gaps between stripes are narrow, the second resist film can be made thin. This shortens the etchback time. Figure 6 [not reproduced] is a cross-sectional SEM photograph showing the condition following application of the method will be discussed. In the resist etchback method described above, the final flatness characteristics are determined by a ratio of the stripe pattern width and the gap between stripes. Therefore, it is better to use a smaller gap; but due to the limitations of resolution, the process window becomes narrow. The oxide film etchback method can be used to avoid this problem. In this method, the oxide film etching depth determines the ultimate surface condition. Figure 8 [not reproduced] shows the structure following oxide film etching and after SOG application. As a result, surface roughness can be decreased up to about 10 percent compared to the condition prior to planarization.

4. Conclusion

The advantage of this technique is that a stripe pattern can be formed automatically at the bottom of the step by utilizing the resist defocus exposure characteristics in a reverse manner. Tests have been done in the past by forming a dummy insulating film pattern in wide gaps between actual LSI wire patterns. However, the CAD support needed to automatically generate the dummy pattern to match each LSI wire pattern is relatively complex, and a dummy pattern mask would be needed for each individual product.

On the other hand, when the new technique is used, once a simple stripe pattern mask is achieved, it can be used for all other products of the same generation, since theoretically the device structure is fixed for each generation (e.g., 0.35μm generation). Also, no new process equipment is needed, and this technique will be relatively easy to implement on a practical basis.

Acknowledgments

This report was based on results achieved by Y. Matsubara, Noguchi, Okumura, Akimoto, and Iwasaki of the NEC ULSI Device Development Laboratory.

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Planarization by Ultrafine Polishing

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1. Introduction

As the VLSI becomes more highly integrated, the device structure is becoming more three-dimensional, and there is a tendency for surface roughness to increase. For example, when considering the development of super-LSI on the level of 256Mbit or 1Gbit DRAM, it is clear that it is necessary to proceed toward thinner films to achieve ultrafine patterning and lower capacitance and resistance in order to achieve faster operational speeds, and to combine (in levels) devices such as Bi-CMOS and three-dimensional devices.

To do so, it is essential that the rough surface be flattened during one of the manufacturing process steps. This process is called planarization, and various methods have been tested. However, use of current planarization techniques, such as reflow/etchback (RIE, etc.) in the processing of VLSI devices, is expected to be extremely difficult to use in achieving the global planarization that is needed for 1Gbit generation devices, and a new approach is needed.[1]

Given this background, ultrafine fabrication techniques such as ultrafine grinding or polishing, with proven results on silicon wafers, have become the focus of attention, and can be regarded as a candidate for planarization technology. In particular, the Elid mirror surface grinding technique[2] developed by Omori, Nakagawa, et al., has drawn attention by being very instrumental in achieving higher precision and definition on silicon wafers. Also, ultrafine polishing takes place during the final steps of silicon wafer manufacture, and mechano-chemical polishing is normally used. Surface roughness reaches about 10 Angstroms Rmax or less, because use of this technique enables a completely smooth mirror surface. From a different point of view, global planarization techniques which use ultrafine mechanical fabrication methods have been used for dielectric isolation (DI) substrates,[3] and SOI substrates,[4] with proven results.

Based on this background, the Nakagawa (Tokyo University) and Doi (Saitama University) research groups have been studying device planarization by ultrafine mechanical fabrication techniques.[5] On the other hand, since IBM Corp. of the United States has reported a planarization method by chemical-mechanical polishing (CMP),[6] Japanese researchers have also started studying this method as a good candidate for planarization.

This report will first give an overview of the planarization of device wafers, and then focus on the ultrafine polishing technique and test equipment and the associated planarization which is achieved.

2. Planarization Techniques for Device Wafers

2.1 Former Planarization Methods and Their Problems

The device wafer planarization techniques used to date can be roughly classified into four types.

Etchback methods, such as sputtering and plasma etching, are relatively simple processes, but there is difficulty in controlling the etching. In *film growth methods*, such as (RF) plasma CVD and Bias-ECR, planarization is performed at the same time as film growth, so there are risks associated with damage and dust. *Fluidization methods*, such as reflow and SOG (spin-on-glass), are easy to use, but film quality is rough, or unstable, and there is a tendency for migration to occur. Other *selective growth* methods, such as the selective CVD/plug method, only require the embedding of necessary parts (holes), but it is difficult to control the selective growth, and factors associated with instability cannot be denied.

The appropriate use of these methods varies depending on the type of film used (e.g., metal film or insulating film), and it has been pointed out that the area which can be planarized is narrow, ranging from a few to 10 microns.

2.2 Expectations and Reported Examples of Planarization by Mechanical Polishing

Most of the methods described above can be called local planarization methods. That is, only the device pattern or crowded areas are planarized, and this does not always eliminate the roughness of the sublayer.

However, the drop in focal depth associated with ultrafine patterning and multilevel structure is becoming serious, and global planarization over the entire wafer level must be achieved for the LSI chip. Planarization by mechanical type polishing has become the center of attention as an effective way to improve the focus margin. In general, planarization in device processes involves the following:

1. Planarization of interlayer insulating film
2. Planarization of metal wire films (Al, Cu, W, etc.)
3. Planarization of SiO_2 in trench isolation structures.

With regard to these, a number of planarization methods which use mechanical-type polishing have been proposed. Although details will not be discussed here, typical examples are as follows:

(1) (Dual) Damascene Method by CMP (Chemical-Mechanical Polishing)[6]/U.S. IBM Corp.

Wire in the shape of a groove is formed on the insulating film, and a Cu thin film is deposited on top. The upper Cu is removed by CMP (chemical mechanical polishing, or so-called mechano-chemical polishing) to form an embedded wire.

(2) Planarization of Interlayer Insulating Film by NMP (Nitride Masked Polishing)[7]/NEC

For insulating films in low circuit regions, silicon nitride film is formed, and serves as the polishing stopper.

(3) Planarization of Interlayer Insulating Film by Polishing[8]/Fujitsu Laboratories

In this method, polishing while suppressing the occurrence of cracks is performed to planarize CVD oxide film and achieve four-layer aluminum wire structure.

2.3 Planarization and Polishing Equipment Currently Used in Mass Production

Although there are many issues which remain to be studied with regard to planarization by mechanical type polishing, this has actually been used in device processes. In particular, the United States has apparently taken the lead in using this method for devices at the 0.5 to 0.8μm level.

Polishing equipment for planarization has been marketed by various equipment manufacturing companies. Table 1 is based on information extracted from catalogs or by oral reports from the various companies.

The specifications and objectives of each device are given below:

- Wafer size: 4-6" diameter or larger (up to about 8" diameter)
- Wafer handling: cassette to cassette (completely automated)
- Method of process completion detection: time-controlled
- Throughput: matches stepper capability (20-30 wafers per hour)
- Environment: appropriate for use in clean room
- Process precision: +/-5 percent of goal
- Cleaning: capable of being linked to automated cleaning equipment

Table 1. Currently Marketed Polishing Equipment and Associated Specifications for Planarization in Mass Production Systems

Name of Manufacturing Company	Cybeg System	Fujikoshi Machinery Industrial Co. (Ltd.)	PRESSI	Speed Fam Co.	Sumitomo Metal Industrial Co. (Ltd.)	R. Howard Strausbaugh Inc.	Westech System Inc.
Model Name	3900	2PD-150	Mechapol E2000	CMP-V	SP-4000	6DS-SP	372M
Dealer	Mitsubishi Materials (Ltd.)	Daito Shoji (Ltd.)	Cosa-Liverman (Ltd.)			Inotech (Ltd.)	Tokyo Electron (Ltd.)
Wafer Size (inches)	φ5", φ6", φ8"	φ6"	φ5", φ6", φ8"	φ5", φ6", φ8"	φ6", φ8"	φ4", φ5", φ6", φ8"	φ4", φ5", φ6", φ8"
Throughput (wafers per hour)	20 to 100 wafers per hour (this varies greatly depending on the process conditions set, and cannot be shown here)						
Method of Process Completion Determination	Controlled by the process time (a fixed process time is set)						
Accuracy (%)	From +/-5 to +/-10 percent of the target value (due to varying residual amounts after processing)						
Batch (number of wafers processed at one time)	6	2	2	1 to 5	5	2	1
Wafer Handling	Cassette to cassette	Cassette to cassette	Cassette to cassette	Cassette to cassette	Cassette to cassette	Cassette to cassette	Cassette to cassette
Polishing Plate	φ36" (φ914mm)	φ400 (mm)	Dual			φ28" (φ710mm)	Dual
Plate Material	Stainless steel	Stainless steel	Aluminum (optional: SUS, granite)		Stainless steel	Granite	Aluminum
Plate Rotation	10 to 32 (rpm)	40 to 400 (rpm)	10 to 150 (rpm)		20-120 (rpm)	10-250 (rpm)	to 200
Head Rotation	10 to 32 (rpm)	40 to 400 (rpm)	10 to 150 (rpm)		30 (rpm)	0 to 260 (rpm)	to 100 (g/cm^2) [sic]
Process Pressure	100 to 700 (g/cm^2)	to 400 (g/cm^2)	100 to 1100 (g/cm^2)		0 to 1000 (g/cm^2)	100 to 700 (g/cm^2)	to 450 (g/cm^2)
Type of Head	Floating head (diaphragm)	Plate-following type	Programmed control type		Sequence control	Programmed control	Counterbalanced type
Polisher (pad) Dressing	Programmed control	Programmed control	Programmed control type		Yes	Programmed control	Programmed control
Polishing Agent (slurry) System	High pressure circulating system	Dual system, low pressure	Dual system, low pressure system	Dual system control type	Circulating system	Dual system, low pressure	Dual system, low pressure
External Dimensions of Equipment	2480 x 1880 x 2460 (mm)	2500 x 1300 x 1600 (mm)	3500 x 2000 x 1900 (mm)	1900 x 3405 x 2260 (mm)	2000 x 1700 x 2000 (mm)	2540 x 1830 x 2030 (mm)	1710 x 2010 x 2360 (mm)
Weight	1930 (kg)	2000 (kg)	2600 (kg)	4500 (kg)	3800 (kg)	3410 (kg)	3338 (kg)
Price	¥35 million to ¥200 million (this varies by manufacturer depending on which peripheral equipment and options are included, and cannot be shown here)						
Items in Common:	Wafer size is 6" diameter (or 4" diameter) or larger.						
	Wafer handing is "cassette-to-cassette" (completely automated).						
	Process completion is determined by time control.						
	Throughput matches the capability of the stepper (several tens per hour).						
	Installation environment is suitable for use in a clean room.						
	Process accuracy is +/-5 percent of the target value.						
	The equipment can be connected to automatic cleaning devices.						

3. Planarization of LSI Device Wafers by Ultrafine Polishing

In the above paragraphs, the effectiveness and significance of device planarization by mechanical type polishing has been discussed. In order to establish this as a solid technology, it is important to reconsider the items required of planarization, while basing efforts on ultrafine polishing techniques established to date.

With regard to planarization of devices and wafers during LSI processing, *the process margin is extremely small (for example, 0.5 to 1 m), and the device pattern surface within that margin should be carefully considered with regard to achieving a high-precision, high-definition, mirror surface without distortion or contamination.* Removal of the necessary amount from the convex areas on the wafer surface in a uniform manner must take priority to achieve planarization. This differs from the polishing of unprocessed silicon wafers in that the process conditions are extremely stringent.

Some methods which can be used to meet these conditions include the ultrafine polishing method discussed by Mr. Nakagawa previously, the ultrafine mirror Elid grinding method,[2] and ultrafine mirror grinding and lapping by subminiature particles (preliminary name),[9] or a combination of these.

This section will focus on "planarization technology for device wafers using ultrafine polishing."

3.1 Planarization/Polishing Methods and Associated Prototype Equipment[5]

Generally, the process amount V in polishing is expressed as follows:

$$V = k \times p \times v \times t$$

(k: constant determined by process conditions, p: process pressure, v: relative velocity, t: process time)

In order to uniformly polish the device wafer surface, the process pressure within the wafer (p) and the relative velocity (v) should be carefully controlled.

With regard to *equalizing the process pressure (p) within the wafer*, it is first necessary to consider the curvature of the wafer and the thickness uniformity. The bending ω_{max} which occurs when an equally distributed load is applied to the wafer can be expressed as follows:

$$\omega_{max} = (5 + \upsilon)\, pa^4/64(1 + \upsilon)D$$

Here, $D = Eh^3/12(1 + \upsilon^2)$, υ: Poisson's ratio ($\upsilon_{si} = 0.262$), p: unit area load (kg/cm^2), D = bending flexibility, E: Young's modulus ($E_{si} = 1.73 \times 10^6$kg/cm^2), h: thickness (cm), a: diameter (cm).

For example, in the case of a φ4" diameter silicon device wafer, with a curvature of about 50μm (the device surface is convex), the corresponding p is 2.4g/cm^2 (190g total load). This is negligible when compared to the total load which occurs during ordinary polishing.

Therefore, by using the air/water back system (see Figure 2), the wafer curvature can be straightened and, at the same time, an equal distribution of pressure can be assured against the polisher. (Of course, methods in which the polisher surface imitates the curvature (shape) of the wafer can also be used.)

On the other hand, *with regard to the relative velocity V*, since only a submicron amount is polished uniformly (and the former polisher tool plate is not rotated independently at a normal velocity of about 30 meters per minute or more), identical small circular movement orbits can be drawn at any point or position on the wafer. Within the range of v = 0.5 to 15 meters per minute, a motion mechanism which achieves any uniform relative velocity can be used. However, in order to avoid nonuniform abrasion of the polisher, and in order to achieve a uniform supply of polishing agent on the process surface, it would be better to rotate the wafer sample or the plate at a negligible rate rather than to use a small circular motion.

Figure 1 shows a pictorial representation of various parts of the equally distributed pressure and small circular motion based on the above description. Figure 2 [not reproduced] shows a prototype planarization and polishing unit.

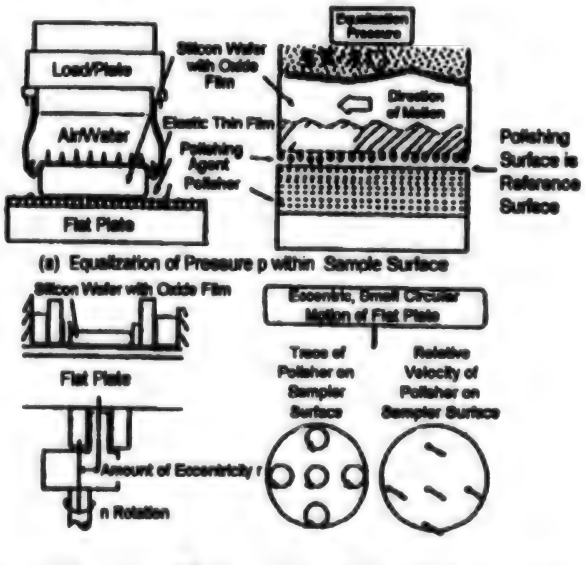


Figure 1. Model Diagram of Precision Equalization Polishing Unit for Planarization

This prototype unit can accommodate φ4" to 6" wafer samples, and processes four wafers equally at the same time. The plate is similar to that described above, and eccentric small circular motions (maximum 60mm diameter, at 100 rpm maximum: in this case relative velocity is 18m/min). Only a slight amount of rotation is applied to the guide ring which secures the sample. In the

equally distributed pressure section, a thin elastic film filled with water or air (for example, silicon rubber 0.1-0.3mm thick) is pressed against the wafer.

Since the polisher greatly affects the planarization of bumps on the surface of the device pattern and high definition it should be selected carefully, and its use with polishing agent should also be considered. For example, the authors developed a thin two-layer (hard/soft) polisher to achieve a high precision and high definition smooth surface (patent no. 1731998). It is also important to consider that the device surface is composed of various metal films and insulating films.

Once the properties of the material to be polished have been ascertained, it can be determined whether polishing should be performed by mechanical action or a combination of mechanical and chemical action. In other words, it is important to determine how much chemical action should be added to the polishing agent according to the conditions set. Also, to promote the chemical interaction and achieve a high definition surface, it appears that ultrafine particles of high purity should be suspended in ultrapure water.

In the planarization of the LSI device surface, it is essential to take extreme measures to prevent the entry of contaminants or foreign materials, so the prototype polishing equipment was installed in a newly constructed super-clean room (purity level, class 10), together with related equipment.

3.2 Fabrication Properties[5),10)]

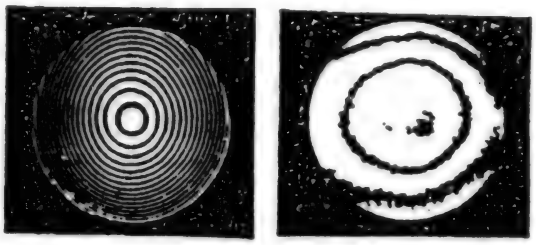
(1) Fundamental properties of the equipment

In this prototype unit, when pressure is added from the rear side of the wafer sample by the water back method, the reference surface is theoretically the polisher surface. In order to check the precision achieved using the prototype unit, the accuracy was first measured without using the water back pressure tool. When this was done, in order to eliminate the effects of elastic deformation and curvature, an experiment was done using a 5mm-thick silicon subs rate. Flatness of about 0.5 μ/φ3" diameter was achieved on the process surface (as shown in Figure 3) and it can be seen that the precision on the polisher surface, which serves as the reference surface of the prototype unit, is relatively good.

On the other hand, in order to confirm the uniform processing of extremely small amounts, an LSI device wafer having a non-uniform surface irregularity (curvature of about 50μ) was selected as the model sample, and planarization was tested using the following conditions: small circular motion radius r = 10mm, rotation n = 50 rpm, and process pressure p = 150g/cm^2.

It was discovered that the elimination amount was uniform over the entire wafer surface, in spite of the fact that there was curvature and unevenness at the initial process stage. This indicates that a uniform process pressure and uniform relative velocity could be controlled with regard to the reference surface (rear side of the polisher). It confirms that the surface oxide film was removed equally even though there was an overall thickness variation of the silicon wafer of about 6μm (TTV).

Precision Check of Prototype Unit (5mm-Thick Silicon Substrate Used; Water Back Pressure Tool Not Used)



(a) Before Polishing (b) After Polishing

Figure 3. One Example of Common Properties Achieved Using the Prototype Unit (Degree of Flatness Before and After Polishing a Silicon Wafer)

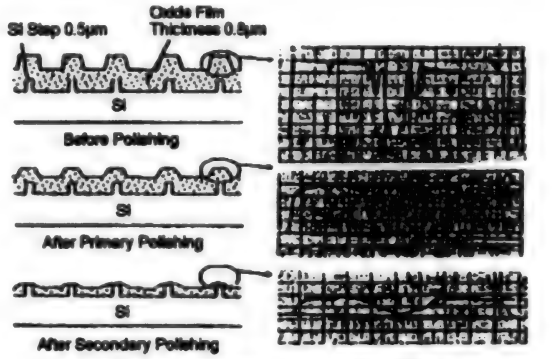
(2) One example of fabrication properties of insulating film (CVD oxide film) with a model pattern[10)]

Figure 4 shows the measurement of residual step differences on a CVD oxide film with a model pattern, for fixed time periods, using the polisher shown in Figure 5, which has a two-layer (hard/soft) construction. For an initial step depth of 0.5μ in the oxide film pattern, the step depth remaining after about 0.4μ of the film was removed was 0.18μ (average), and the variation of removed amounts within the wafer was 0.05μ. The polisher used in this case has proven results related to achieving high precision and high definition on unprocessed silicon wafers. However, it cannot always be used satisfactorily for planarization purposes.

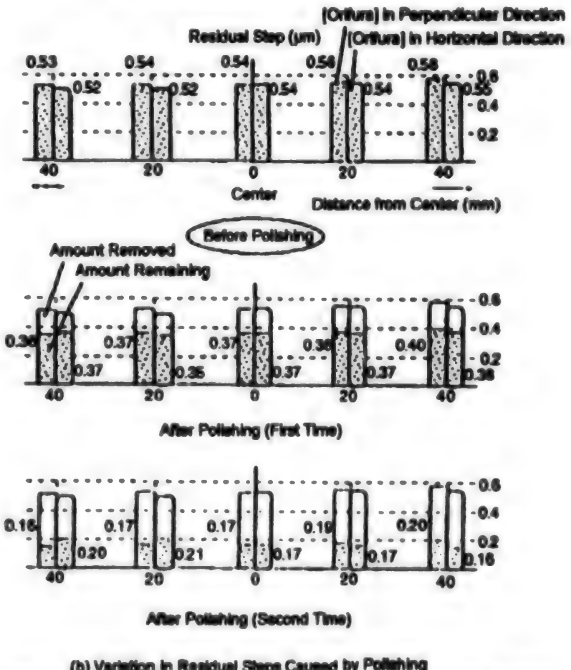
(3) Proposal for polisher to be used in global planarization

As described above, the polisher (polishing pad) has a direct effect on the complete flattening of device pattern surface roughness. The basic conditions are that the convex areas must be removed first, regardless of the pattern size or density; and extreme care must be taken to avoid the concave areas of the pattern.

On the other hand, if the process completion point is controlled and determined by the process time, the process rate must guarantee long life of the polisher and good reproducibility. For the various units on

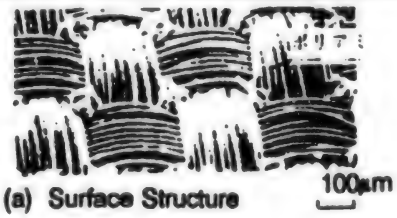


(a) Variation in Residual Steps Caused by Polishing



(b) Variation in Residual Steps Caused by Polishing

Figure 4. Polish Characteristics for Oxide Film With Model Pattern



(a) Surface Structure

Figure 5. Hard/Soft Two-Layer Polisher

the market shown in Table 1, in order to achieve a reproducible process rate, a dressing tool is provided for the polisher and the polisher is renewed at fixed time intervals.

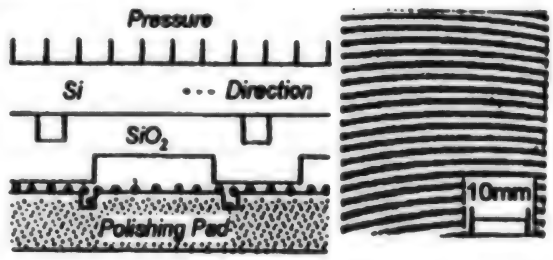
The two basic conditions for polishers used in global planarization are:

(a) Appropriate hardness (especially the surface)

(b) Constant and uniform supply of processing agent (polishing agent) to the surface of the sample, and a concave area for disposal of the process remnants.

Condition (b) assures a reproducible process rate, and is important in preventing the occurrence of clogging. In order to accomplish this, it was thought that it would be better to use a polishing pad which did not contain fine pocket-shaped holes in the polisher surface (conventional wafer polishing uses pads with this type of holes). However, since the process agent must be maintained and the process remnants must be removed, it is better to use a continuous groove rather than small closed holes. When the process surface which comes in contact with the sample is a smooth and flat surface which does not have small holes, the convex areas on the device wafer are removed consecutively to achieve planarization, and clogging does not occur. Therefore, a special dressing is not needed.

Keeping the above in mind, a polisher which has a high elastic deformation ratio E and cross-section coefficient I (Model I) was conceived and a prototype was assembled. (See Figure 6.)



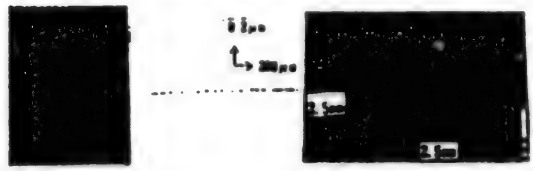
(a) Planarization Model by Special High EI Polisher

(b) Photograph of Polisher Surface

Figure 6. High EI Polisher (Model-1) Developed for Global Planarization

Figure 7 shows an example where the oxide film was removed 0.5μm from the surface, using the prototype unit (Model I). It was shown that the remaining step difference was 0.01μm or less, in spite of the pattern sizes (step depth 0.5μm; width 300, 200 and 500μm; and length 1mm). Variation of the remaining step depth within the wafer was also within 150 Angstroms, and this can essentially be regarded as global planarization. (See Figure 8.)

Before Processing, (a) Surface, (b) Cross Section, (c) Three-Dimensional Shape



After Processing, (a) Surface, (b) Cross Section, (c) Three-Dimensional Shape

Figure 7. Planarization of Patterns by Special High EI Polisher

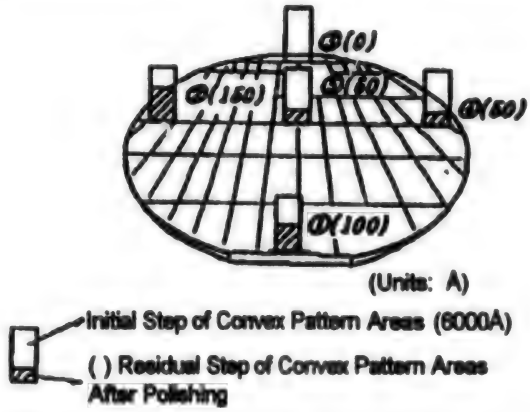


Figure 8. Process Amount and Distribution of Residual Steps in Wafer (Polish Characteristics of Device Wafer)

In this report, the possibility of implementing ultrafine polishing technology for planarization of LSI device/wafer has been discussed. A prototype planarization/polishing unit for high precision applications was designed and assembled. As a result, it was shown that there is a favorable outlook for uniform planarization and polishing over the entire surface of the LSI device/wafer.

4. Conclusion and Future Research Topics

In this report, the possibility of using ultrafine polishing technology in the planarization (flattening) of silicon device wafers was examined, and the features of planarization units on the market were presented. In consideration of these units, since the application of ordinary polishing equipment was acknowledged to be difficult, new equipment specifically for planarization was designed. The results of processing achieved by the new equipment show that it is effective for global planarization of device wafers.

Polishing technology requires a significant amount of "know-how," so it is important to carefully scrutinize the mutual interactions which take place among the material being processed, the subminiature particles, and the polishing agent; and to discover what mechanisms these interactions are based on. It is necessary to confirm the electrical properties and find the global planarization conditions which can be used in device processes, in conjunction with examining the relevant process methods and equipment, the environment in which the equipment is to be installed, the elimination or cleaning of contamination and particulates, and the method used for detecting the completion point of polishing.

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Planarization Technology—New Testing of Polishing Machines and Polishing Pads

94FE0802F Tokyo JAPAN SOCIETY FOR PRECISION ENGINEERING in Japanese 16 Jun 94 pp 17-21

[Lecture by Junji Watanabe, Sumitomo Metal Industrial Co. (Ltd.), Semiconductor Equipment Group]

[FBIS Translated Text]

1. Introduction

Multilevel wiring technology has become essential in conjunction with the subminiaturization and higher levels of integration in LSIs. Three to five levels of wiring are now being used in logic LSIs, where numerous and complex wiring is required between devices.

To achieve good reliability and high yield in multilevel wiring, the interlayer insulating film between layers must be flattened. In the past, shaping techniques consisting of various types of CVD methods, or a combination of CVD and etching, were used for planarization. However, complete planarization over the entire surface of the wafer could not be achieved.

Since IBM announced the success of chemical mechanical polishing (CMP) for interlayer insulating film and metal wire, CMP has become the focus of attention for possible use in LSI processing. CMP of interlayer insulating film not only achieves a global planarization which cannot be achieved using other methods; it is a very effective technique which simplifies processing and is associated with lower cost and is already being used on a practical basis in the United States. However, there are still many problems which need to be examined, such as the compatibility of pre- and post-dry/clean processes, precision and reproducibility of planarization, and the effects on electrical properties of the insulating film after CMP is performed.

In this report, the chief factors involved in polishing technology with regard to CMP planarization of insulating film, and related examples and problems will be discussed. This includes the polishing pad, slurry, and polishing machine.

2. Requirements for Planarization and Polishing of Interlayer Insulating Films

Film characteristics of interlayer films differ depending on the source materials used (such as gases) and the formation method used (such as CVD); therefore, the polishing requirements also vary. In order of polishing rate, there is BPSG film, O_3-TEOS film, PE-TEOS film, and ECR-CVD film. The latter two have about the same polishing rate; the polishing rate for O_3-TEOS film is 20-30 percent faster, and the rate for BPSG film is two to three times faster than ECR-CVD film.

Pattern shapes in interlayer films differ according to the device structure, and there is no specific shape. Also, depending on the method used to form the interlayer film, when patterns are completely embedded between wire layers, a linked pattern is formed and in some cases there are wide lines 0.5mm-1mm in size. Therefore, a planarization and polishing method which allows for L&S (lines-and-spaces) varying from the submicron level to millimeters is needed.

The thermal expansion coefficient of interlayer film is small compared to the silicon substrate; so at normal temperatures there is a residual stress (compression) on ordinary films, and a convex curvature of 12-20 or 30 microns occurs on the film formation side of the substrate. There is also a difference in the thickness of the substrate itself, which ranges from several to 10μm for 6" or 8" wafers.

The following objectives are important for the interlayer film described above: flatness over the entire substrate should be within 0.1 to 0.2μm; uniformity of residual film thickness within the substrate should be within +/-5 percent; high throughput should be achievable at a polishing rate of 1500 to 2000 Angstroms per minute; and reproducibility from lot to lot should be within +/-5 percent.

3. Factors Involved in Planarization and Polishing Technology for Interlayer Insulating Films

3.1 Polishing Pad

Tools represent the most critical factor in high precision fabrication technology. In polishing technology this means the pad and the slurry. Requirements of the pad for planarization and polishing of interlayer insulating films are that it should follow the thickness variations and curvatures over the entire original substrate and selectively polish only the convex areas of subminiature patterns. Also, good reproducibility should be achieved at a high polishing rate. In current technology, there is no clear method of detecting the polishing completion point with high accuracy during the polishing process, so it is extremely important to achieve reproducibility of the polish amount relative to the polish time. Varying factors associated with the polish amount include clogging on the pad surface caused by the slurry and fluctuation in the elasticity based on this clogging. Therefore, it is important that there should be little variation in the physical properties of the pad surface.

In the effort to optimally reduce the roughness of the polishing surface, if a soft foam polyurethane pad (used for polishing silicon substrates) is used (as shown in Figure 1), the pad will change shape according to the polishing pressure; it follows the convex and concave areas of the pattern on the interlayer insulating film surface, and the concave sections are polished as well as the convex sections. Efficiency of planarization is thus low and complete planarization cannot be achieved. On the other hand, if only the convex sections are selectively polished, and a very hard pad is used, there is little elastic deformation, and only the high areas associated

with variation of the original substrate thickness (substrate TTV) and curvature are polished (see Figure 2). The polish distribution over the entire substrate becomes non-uniform, and polishing cannot be performed using surface shape as the reference.

Figure 1. Schematic View of Planarization by Conventional Soft Pad

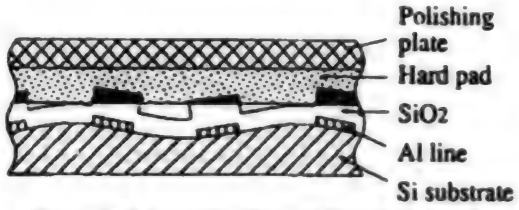


Figure 2. Schematic View of Planarization by Conventional Hard Pad

A special type of pad construction is needed in order to selectively polish the convex areas of subminiature patterns on the surface of interlayer film, and to achieve a uniform amount of polishing over the entire surface by following substrate thickness variations and curvature. Figure 3 shows one example of this type of construction. The part which touches the surface being polished is a resin consisting chiefly of hard polyurethane rubber, and this part is divided into square shapes. These hard pieces are positioned in a soft elastic material. The hard resin parts also have very few air holes. When this type of pad is used, the capability described above can be easily achieved. Since there are few air holes, there is little clogging associated with the slurry and minimal fluctuation in the polish rate. The slurry can be easily supplied to the polish surface through the gaps between the hard resin parts.

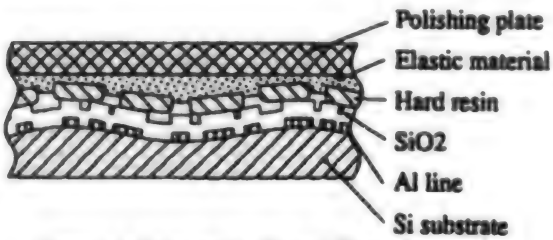


Figure 3. Schematic View of Planarization by Developed Pad

3.2 Slurry (polishing agent)

It is known that SiO_2 film easily bonds with OH radical in a weak alkali solution at high pressure and lower temperature, and becomes elusion by hydration. With the mechanical abrasion of subminiature particles within the slurry, high temperature and high pressure occurs locally, and the activated surface bonds with the OH radicals to form a fragile reactant, which is removed by the mechanical action of the particles which takes place, thus resulting in the polishing mechanism.

In order for the action of the small particles to be uniform over the entire surface, it is necessary that the particles are well dispersed in the polishing solution and that the particles are of uniform diameter. To achieve planarization of large, small, and rough patterns, particle diameter should be 0.1μm or smaller. Colloidal silica meets these conditions best. However, when colloidal silica slurry is used, it gels and becomes glass-like when dried. A small piece of this could cause scratches and damage if it were present during the polishing process. Colloidal silica created by ordinary hydrolysis and so-called "fumed silica" which is formed by flame hydrolysis is also used. At present, the latter type is frequently used because it has a high polishing rate and gels easily.

3.3 Polishing Machines

The mechanism of the polishing machine is important to achieving a steady polish rate and uniform polishing over the entire substrate surface, with good reproducibility and high throughput.

Figure 4 shows the mechanism of an ordinary machine which has an arm for holding the substrate on a rotating plate. Polishing is accomplished while turning or rocking the wafer. In this system, the reference surface for polishing is the polishing pad on the polishing plate, and the shape of the pad surface is transferred. Although there is only one or two heads in the wafer holding section of conventional machines, some units which have five or six heads have been developed to achieve higher throughput.

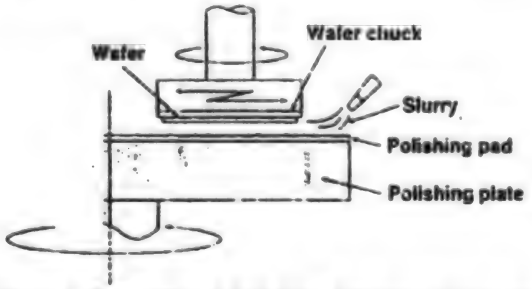


Figure 4. Conventional Polishing Machine Mechanism

Figure 5 shows the basic structure of a new polishing machine which processes five wafers simultaneously. Each of the five wafers is situated on a stage with each stage rotating in conjunction with a large table which serves as the reference. The flat surfaces of the polishing plates are stacked on top of a surface which is comprised of the five wafers being polished, and then rotated. In other words, a stable polishing mechanism is achieved by arranging each of the wafers as a part of a larger substrate. Uniformity of the polish conditions is enhanced because the position of the wafer at any point inside the machine and the positions relative to the polishing plate are not fixed. Therefore, the five substrates are processed under identical polish conditions, and uniformity within lots, as well as reproducibility and uniformity between different lots can be easily assured.

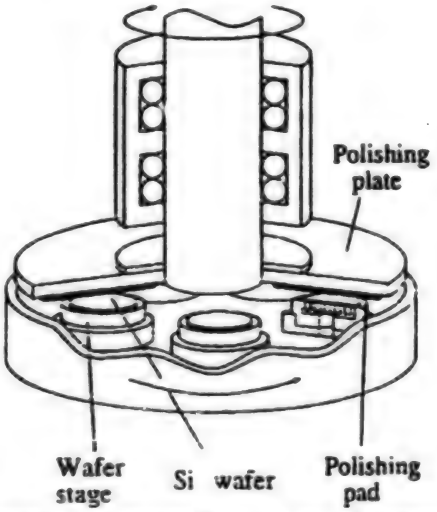


Figure 5. Schematic View of CMP Equipment

The five adhesion tables which serve as the reference, and the large rotating table underneath, are highly rigid; precision movement is guaranteed even during high speed rotation with a high load. At present, there is no effective method of detecting a completion point when polishing insulating film with circuit patterns. Unless the method or equipment can assure reproducibility of the polishing rate, it cannot be used for mass production applications. It is very important to select a polishing method which has high reproducibility.

4. Planarization and Polishing Interlayer Insulating Films

An actual example of planarization/polishing of interlayer insulating films using the polishing pad, slurry, and polishing machine described above, will next be described.

Figure 6 shows an example of planarization/polishing of a model pattern. For pad A, the concave areas in wide spaces are polished, and it is difficult to reduce the step differences. However, with pad B, the convex areas are polished selectively even for wide patterns 0.5 to 1mm in size. It can be seen that conditions converge at a step difference of 0.2 to 0.2μm or less. Pad B uses a polyurethane rubber that is harder than pad A.

Figure 7 shows raw data for the polish distribution at various parts for a wafer having a curvature of 10-20μm. Uniformity of polishing is within +/-5 percent except for 8mm at the periphery of the wafer. The elasticity of the hard/elastic material in the outer periphery has not been optimized (see Figure 3). This is a subject for further research.

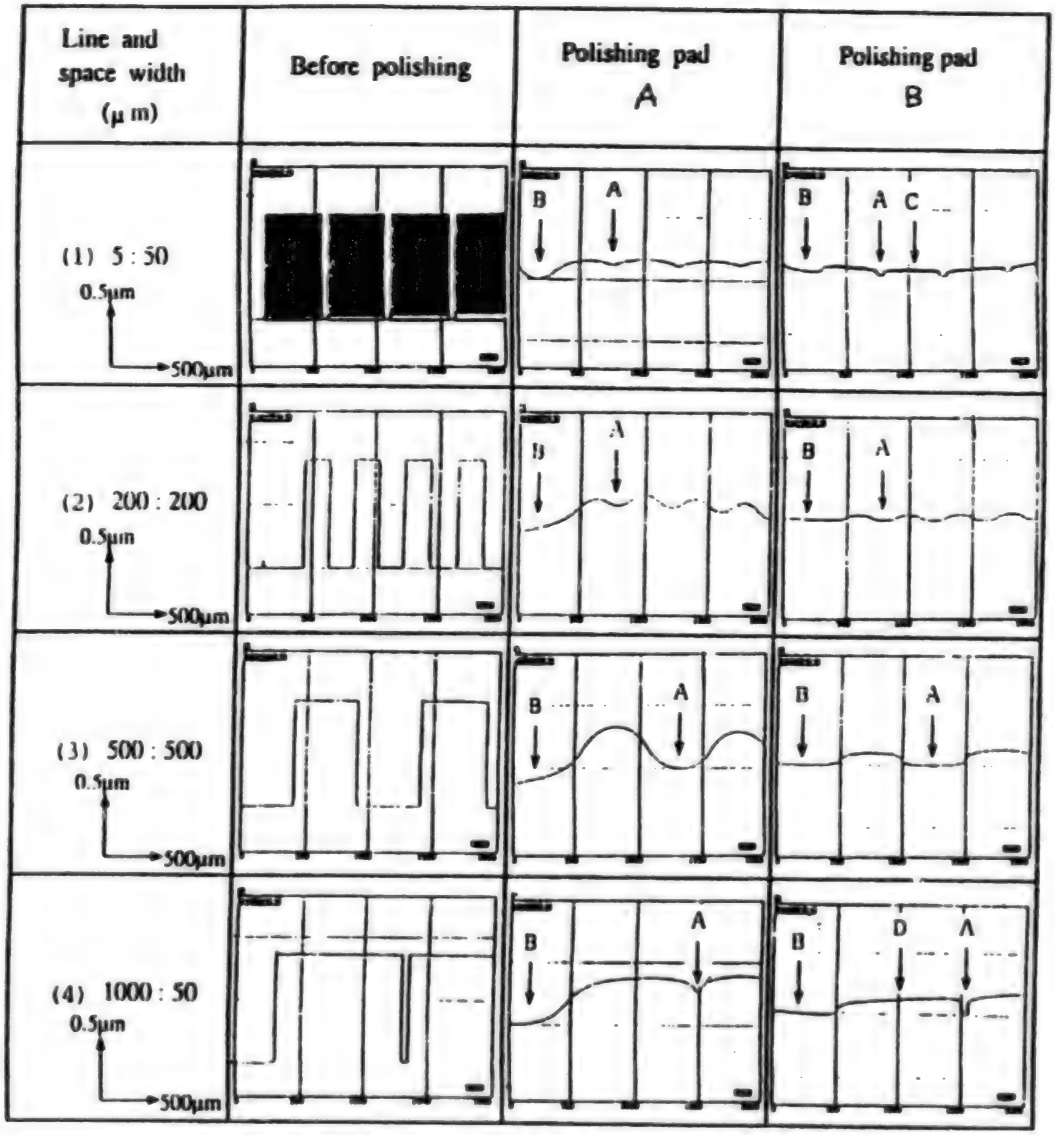


Figure 6. The Dependence of Polishing Rate on Pattern Width

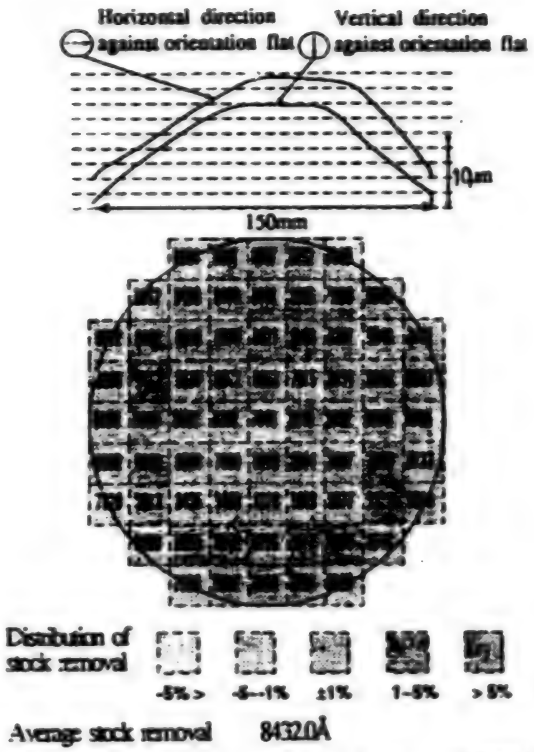


Figure 7. Uniformity Map for Stock Removal Within Wafer Warped About 15μm

Table 1 shows the polish amount and distribution for each wafer when five wafers are polished simultaneously. Variation in the polish amount is within 2 percent for all five wafers, and the polish amount distribution is also within +/-3 to 5 percent for each wafer.

Table 1. Typical Uniformity Data Within Polishing Stage

Stage No.	Average Polishing Amount (Angstroms)	Distribution (%)		
		+/-10%	+/-5%	+/-3%
St.1	9885.6	100	100	92
St.2	9676.3	100	100	100
St.3	9800.6	100	100	96
St.4	9745.8	100	100	100
St.5	9805.5	100	96	92

Figure 8 shows data for the permissible difference in wafer thickness of the five wafers being simultaneously polished. It indicates a clear difference in polish amount when the thickness is over 40μm. Normally, the thickness of a 6" wafer is regarded to be +/-20μm, but in reality all wafers are +/-10μm, so there is no need to separate wafers according to thickness when this polishing method is used.

Figure 9 shows the variation in polishing pad life and the polish rate. The slurry is recirculated in this system, so it

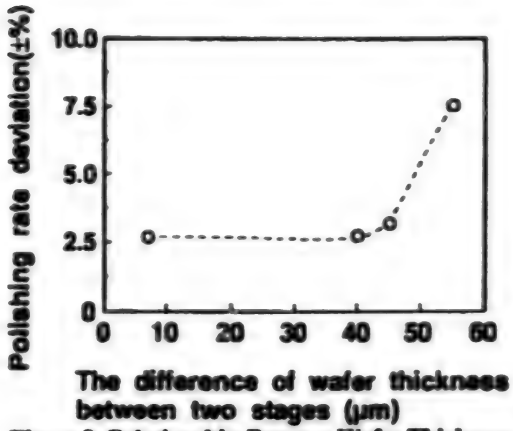


Figure 8. Relationship Between Wafer Thickness Difference and Polishing Rate Deviation

is necessary to establish the slurry lifespan. After about 10 hours of use, the rate drops sharply. This is considered to establish the slurry lifespan, and testing was done within this time range. The results indicate that the rate variation, when using the pad continuously, is only about 30 Angstroms per hour, and the pad can be used more than 10 hours. In this testing there was absolutely no conditioning done to the pad. The reason for the gradual increase in polishing rate in Figure 9 is not clear, and it is necessary to further suppress the variation.

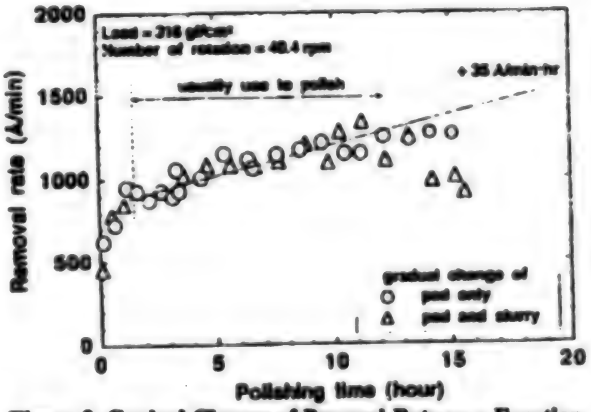


Figure 9. Gradual Change of Removal Rate as a Function of Total Polishing Time for Pad and Slurry

5. Conclusion

Planarization and polishing technology and equipment have been developed for the interlayer insulating films which are used in the processing of multilevel wires for ultrafine LSIs. High performance polishing systems have been achieved using different types of polishing pads and polishing machines. However, at the same time, the patterns on the interlayer films differ depending on the device structure or design, and the types of problems which may arise in the future cannot be predicted. The cleaning technique following polishing, and the electrical

properties of the film after polishing have also not been established. Future efforts will also be directed toward achieving better equipment based on application in actual devices and further evaluation.

Post-Treatment Wafer Cleaning Techniques and Equipment

94FE0802G Tokyo JAPAN SOCIETY FOR PRECISION ENGINEERING in Japanese 16 Jun 94 pp 22-25

[Lecture by T. Eitoku of Dainippon Screen Mfg. Co., Ltd., Yasu Plant]

[FBIS Translated Text]

1. Introduction

Chemical-mechanical polishing (CMP) technology has recently become the focus of study for its applications in planarization of LSIs. CMP technology has been examined for use in planarization of interlayer insulating films in LSI production processes, for multiple layer embedding of metals, and a number of other applications. There is also a wide range of materials which can be polished; this includes metals such as oxide films (SiO_2), aluminum, and tungsten, as well as poly-Si and SiN.

However, when efforts are made to use CMP in LSI production processes, post-processing cleaning becomes a problem. Since a slurry consisting of colloidal silica or other materials is used as the polishing agent in CMP, a large number of particles remain on the wafer surface after CMP is done. (See Figure 1.) Also, the polishing agent frequently contains KOH and NaOH. These and other metal impurities contaminate the wafer surface. (See Figure 2.) To eliminate these particles and metal contamination which are serious threats to LSI production processes, a post-treatment cleaning is needed.

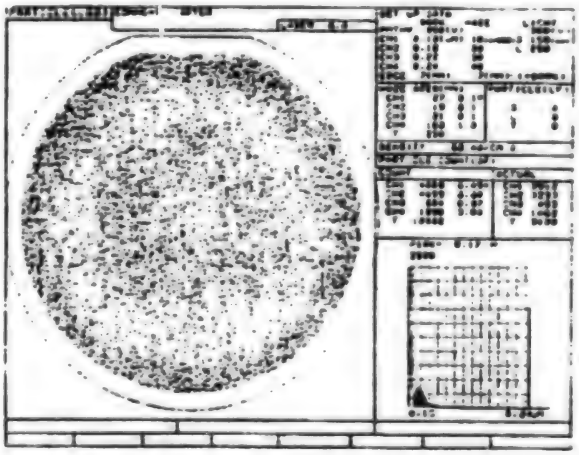


Figure 1. Particle Map Following Chemical Mechanical Polishing

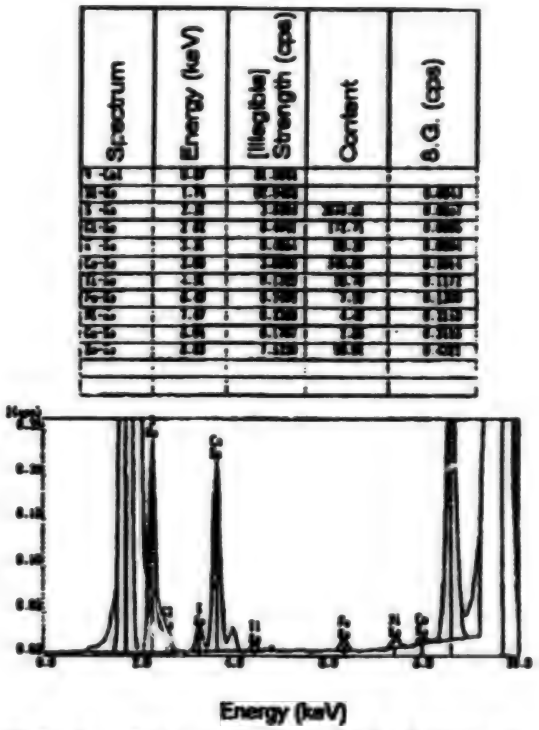


Figure 2. Analysis of Metals on Wafer Surface After CMP

This report will cover post-polish wafer cleaning methods, cleaning equipment, and cleaning results.

2. Condition of Wafer After CMP, and Objectives of Cleaning

(1) Particles

Several ten thousands of particles (16μ or larger in size) are normally observed on the wafer surface after polishing. Most of these particles are thought to be polishing agent, but there could be fragments of the polishing pad or other types of particles.

These particles can be removed to some extent by rinsing with water, but for LSI production processes, a separate cleaning must be performed.

Removal of these particles is the primary object of cleaning after CMP processing, and a cleaning device with high particulate removal capability is needed. After polishing, if the wafer is dried completely, the particles become difficult to remove, so it is necessary to use a method whereby the wafer does not become dry until after the cleaning process is done.

(2) Metal contamination

As described above, KOH and NaOH are frequently contained in the polishing agent, and the wafer surface becomes contaminated by these and other

metal impurities. Figure 2 shows the results obtained from a total reflection fluorescent X-ray analysis (TXRF) of the wafer surface after polishing oxide film.

In addition to K, other metals, including Ca, Fe, Zn, were detected at 10^{10} to $10^{12}/cm^2$. The objective of the cleaning equipment is to remove these metal impurities.

3. Cleaning Equipment for Use After CMP

The following objectives are required of equipment that is designed to clean wafers after polishing.

1. It should have a high particulate removal capability.
2. It should be able to completely remove metal contamination.
3. It should be compact and easily configured into the polishing unit (and it should be capable of in-line use).
4. To increase the cleaning effect, the wafer should not be dried until after cleaning is completed.

Table 1 shows the cleaning methods and features for various types of cleaning equipment designed for use after CMP.

Table 1. Post-CMP Cleaning Units

Cleaning Equipment	Cleaning Method	Advantages	Disadvantages
Batch-type cleaning unit	NH_4OH/H_2O_2 DHF H_2SO_4/H_2O_2	High throughput	Large footprint Risk of cross-contamination Large amount of chemical used Limited selection of chemicals
Single wafer spin cleaning unit	Ultrasonic cleaning NH_4OH/H_2O_2 DHF H_2SO_4/H_2O_2	Small footprint Clean chemicals	Limited selection of chemicals
Single wafer scrub clean unit	Scrub cleaning Ultrasonic cleaning	Can remove particles	Cannot remove metal contamination
Single wafer scrub and chemical cleaning unit	Scrub cleaning + DHF Scrub cleaning + NH_4OH/H_2O_2	Small footprint Small amount of chemicals used Can remove both particles and metals	

In the case of multiple tub, immersion type batch cleaning unit, which has been widely used in the past, many wafers can be cleaned at one time, and throughput is high. However, it requires much space, and cannot easily be configured into the polishing unit. In addition, cross contamination is a risk between wafers and batches, and frequent chemical exchange can be expected.

Scrubbers which use brushes and sponges have been used in the past for removing particles. Scrubbers can remove the particles, but are not desirable for removing metal contamination.

As a post-CMP cleaning unit, Dainippon Screen has proposed a single wafer scrub and chemical cleaning unit which provides the scrub cleaning function as well as the chemical cleaning function. This unit provides the synergistic effect of scrub cleaning and chemical cleaning to achieve high particle removal capability, and also chemical cleaning to remove metal contamination. Since scrub cleaning and chemical cleaning can be done within the same chamber, the unit requires little space, and it can be easily configured into polishing equipment layout.

4. Scrub and Chemical Cleaning Equipment

Figure 3 shows the composition of the scrub and chemical cleaning unit "SP-W813-AS" developed by Dainippon Screen. The unit consists of three chambers—a rear side scrub chamber, a surface scrub and chemical spray chamber, and final rinse and spin dry chamber.

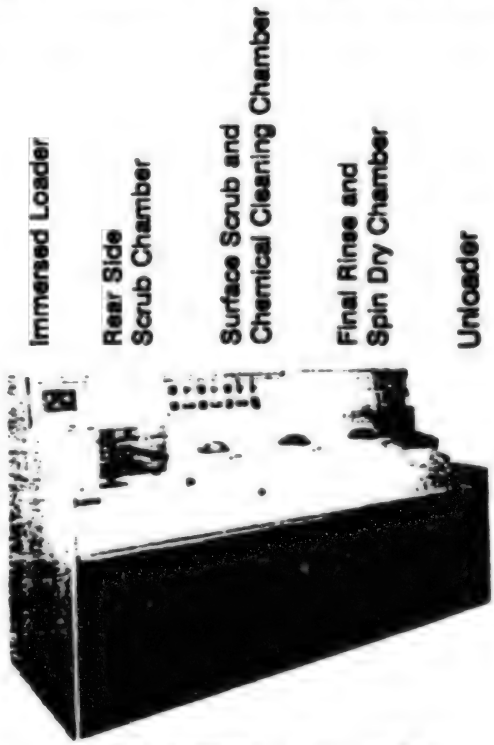


Figure 3. SP-W813-As External View

For the surface scrub treatment, a rotating brush which has a high particulate removal capability is used. The brush can easily be replaced or serviced. To prevent

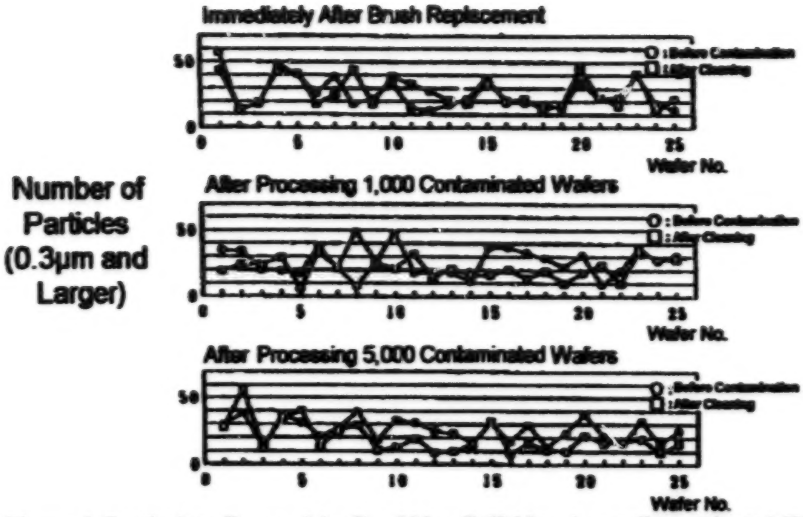


Figure 4. Particulate Removal by Scrubbing Polishing Agent Contaminated Wafer

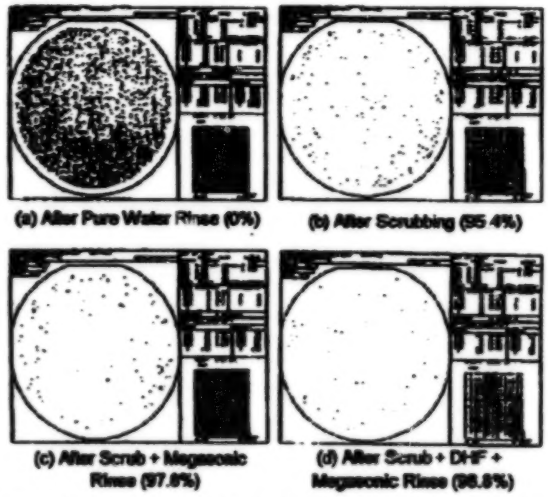
drying, the wafer is kept in a submersed loader until cleaning begins. In the rear scrub chamber, a special brush is used to remove particles adhered to the rear surface. A chemical nozzle is situated in the surface scrub chamber to enable chemical cleaning of the front and rear surfaces of the wafer. The synergistic effect produced by the physical action of the rotating brush and the chemical action of the chemical treatment results in very high performance particle removal, and this removal can be done in a short time. In the final rinse/dry chamber, the final rinse is done using ultrapure water, and the wafer is dried by a high speed spin process. A megasonic spray clean function can also be added.

(1) Particles

Figure 4 shows the results of particulate removal for an 8" oxide film wafer which was contaminated with polishing agent and then scrubbed using the new unit. Stable removal of particles could be achieved even after 5,000 wafers were cleaned.

Figure 5 shows a comparison of scrub cleaning with HF (0.5 percent), and megasonic cleaning, used on a 6" oxide film wafer. Compared to a pure water rinse alone, the particulate removal rate by the scrub was 95.4 percent, when megasonic cleaning was added to the scrub the rate was 97.6 percent, and when HF cleaning was added, the rate increased to 98.8 percent.

Figure 6 shows the cleaning effect on a polished 6" silicon wafer (bare). For a silicon polished wafer, when both scrubbing and SC1 processes are used, almost all of the particles 0.16μ or larger were removed. When the SC1 process was used alone, more than 10,000 particles remained on the wafer, and SC1 cannot be used to remove particles in a



( ) Rate of Particulate Removal with (a) Pure Water Rinse as the Reference

Figure 5. Particulate Removal After Polishing Oxide Film

short time. The number of particles was decreased sharply to seven by adding a scrub process. This indicates the effectiveness of scrubbing in the removal of particles from a polished wafer, and shows that the cleaning effect can be increased even further by adding a chemical cleaning treatment.

(2) Metal contamination

After polishing, the wafer is contaminated with potassium or other alkali metals, or with heavy metals such as iron and zinc. Since these metal contaminants cannot be removed by pure water rinsing or scrubbing, chemical cleaning is essential.

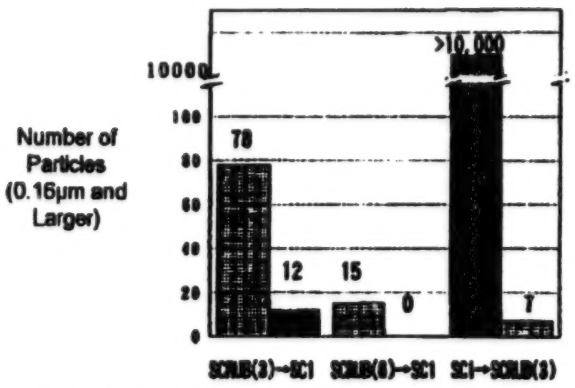


Figure 6. Particulate Removal After Silicon Wafer Polishing [Figures in parentheses indicate the number of scrub repetitions, SC1 = 1:1:10 80°C 1 min.]

Figure 7 shows the results of a total reflection fluorescent X-ray (TXRF) of the metal impurities on the surface of a polished oxide film wafer after cleaning has been done.

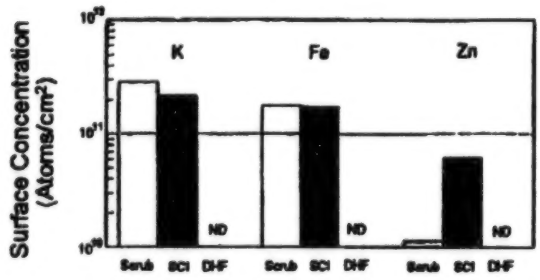


Figure 7. Removal of Metallic Contamination After Oxide Film Polishing

Iron and zinc were detected after the polished oxide film was scrubbed with pure water. Metallic ions could not be removed even after an alkali cleaning (SC1 $NH_4OH/H_2O_2/H_2O$) was performed after scrubbing. Almost none of the potassium or iron was removed, and the concentration of zinc increased. On the other hand, when diluted HF (0.5 percent) cleaning was done after scrubbing, these metals were not detected by the TXRF analysis, and metallic contamination was eliminated to the detectable limit (10^{10} to $10^{11}/cm^2$).

From the above results, it appears that the optimum cleaning method after oxide film has been polished is a combination of scrubbing and diluted HF cleaning. Use of the scrub and chemical cleaning unit "SP-W813AS" developed by Dainippon Screen produces a highly effective cleaning process for both particulate and metallic contamination.

It appears that it is necessary to optimize brushing and cleaning by selecting the proper brush material and type of chemicals used. It also seems that, in addition to optimizing the cleaning equipment and conditions, the polish conditions and the wafer maintenance conditions should be carefully considered from the polishing step throughout the cleaning process to enhance cleaning effectiveness.

5. Conclusion

The importance of treatment and cleaning following chemical-mechanical polishing, and the necessity and effectiveness of both scrubbing and chemical cleaning have been discussed. Testing of CMP techniques in LSI processes is relatively recent, and further progress is expected. In a similar manner, the cleaning equipment used after CMP processing should be further studied and improved in the future.

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